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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,082	11/05/1999	KEVIN J. RYAN	303.306US2	3448

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EXAMINER

PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 09/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/434,082	RYAN, KEVIN J.	
	Examiner	Art Unit	
	B. James Peikari	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5-8 and 29-71 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5-8 and 29-71 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 15 July 2002 is: a) ☐ approved b) ☒ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>15</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The previous objections to the drawings under 37 CFR 1.83(a) are withdrawn in view of a proposed Figure 6 included with the amendment of July 15, 2002. The examiner has reconsidered his position on whether the inclusion of discrete data in and data out buffers associated with an individual DRAM should be considered new matter, for reasons discussed in detail below. Consequently, Figure 6 has been approved for entry by the examiner and is not considered to contain new matter.

2. The previous objections to the drawing under 37 CFR 1.84(p)(5) are withdrawn due to applicant's July 15, 2002 amendment of the specification to correspond to the drawings.

Specification

3. The previous objections to the specification are withdrawn due to the amendment filed July 15, 2002.

Claim Rejections - 35 USC § 112

4. The previous rejections under 35 U.S.C. 112, first paragraph, are withdrawn. The examiner has reconsidered his position upon discovering references that teach that the inclusion of discrete data in and data out buffers associated with individual DRAMs was, although not universal, well known at the time of the invention.

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Applicant's submission of pages 2 and 9 of *DRAM Circuit Design* on January 17, 2002 was not convincing for the reasons stated in section 10(B) of the previous Office action. However, a prior reference (Rosich et al., published in 1996) supporting applicant's assertion that it was well known to include data in and data out buffers with individual DRAMs is included herewith.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5-8 and 29-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al., U.S. 5,875,452, in view of Rosich et al., U.S. 5,587,964.

Katayama et al. teach the claimed invention in a memory system (*note especially Figure 9*) comprising:

a memory controller (*note memory controller 17, via controller 70*) with a unidirectional command and address bus (*note that the address and control lines from controller 70 to the decoders are all unidirectional*),

a bidirectional data bus (*note that data line 56 is bidirectional*), a plurality of memory devices, such as eight, (*note the use of up to sixteen exemplary DRAM devices 22*),

a shared command buffer (*note the registers A and B in controller 70, which are connected to each of the plurality of memory devices 22, as explained in column 26, lines 56-57*) coupled between the command and address bus (18; *note that bus 18 comprises, in part, a control bus and an address bus*) and the plurality of memory devices (22) for receiving and latching commands and addresses, and

a shared data buffer (*note data buffer 78*) connected between the plurality of memory devices (22) and the bidirectional data bus (18; *note that bus 18 comprises, in part, a data bus*) for receiving and latching read data or write data.

As for the claimed pipelined packet protocol, note column 2, lines 34 et seq. and column 20, line 6. [As to the meaning of "pipelined subsystems", it is clear from applicant's specification, page 8, lines 27-30, that this means that each subsystem 130 is pipelined within itself. It does *not* mean that each subsystem is one link in a larger pipeline.]

As for the feature of each memory device containing a column decoder and a row decoder, note column 26, lines 51-57.

As for the feature of each memory device containing a data in buffer and a data out buffer, such was not specifically mentioned in the Katayama et al. system. However the benefits of adding additional levels of buffer hierarchies was well known at the time of the invention. It would have been obvious to include data in and data out buffers for each of the memory devices 22 in the Katayama et al. system. In any case Rosich et al. teaches a DRAM device compatible with the Katayama et al. system and which explicitly teaches a data in buffer and a data out buffer associated with the storage array (note, e.g., Figure 1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the DRAM devices of Rosich et al. as the DRAM devices of Katayama et al., since buffers in the Rosich et al.

DRAM would have made the timing of the transfer operations to and from the shared buffers more efficient (by latching the data, control or address bits so that such protocols as time sharing could be utilized), especially considering the highly parallel nature of the Figure 9 embodiment of the Katayama et al. system.

At this point it is apparent that the above Katayama et al./Rosich et al. combination teach each and all of the features of *one* of applicant's memory subsystems 130.N. On the other hand, each of applicant's embodiments include a *plurality* of such memory subsystems. In the remarks submitted with the amendment filed January 17, 2002, applicant has now clarified the scope of what is meant by "memory subsystem" (when the specification mentions "each memory subsystem 130" it does *not* mean all of the units which start with "130", it really means "each memory subsystem 130.N", i.e. each *one* of the units surrounded by dashed lines). The combination of references recited above does not specifically mention that memory controller 17 could be connected to *more than one* storage device 16. However, the benefits of adding extra memory were quite well known. Whether extra memory devices 16 were added in parallel, series or in some combinations thereof, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add such extra devices to the Katayama et al./Rosich et al. combination since (1) extra memory meant that more data could be stored, (2) several storage devices 16 linked in parallel would have allowed for faster data retrieval via parallel data transfers, (3) it was noted in St. Regis Paper Co. v Bemis Co. 193 USPQ 8 (7th Cir. 1977) that to duplicate parts for multiple effects is *not* given patentable weight, and (4) the suggestion for plural memory devices is *within the Katayama reference itself* (note column 26, lines 30-45) – in this embodiment the DRAM arrays 22 become part of a larger array of up to 16 devices (in column 9, Katayama explicitly states that "it is preferable that the storage

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device has a plurality of the DRAM arrays"); consequently, the same motivations exist for integrating the storage device 90 into a larger array of such storage devices.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 5-8 and 29-71 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4, 26-28 and 32-57 of U.S. Patent No. 6,286,062. Although the conflicting claims are not identical, they are not patentably distinct from each other because each and all of the features of the present claims are included in the claims of the '753 application.

Although the present application is a divisional of the '753 application, and the divisional resulted from a restriction requirement,

- (1) the examiner concedes that claims 26-28 should have been included in group II, as opposed to group I. However,
- (2) it is noted that *after* the restriction requirement was made, applicant never amended the claims 26-28 to be consonant with the restriction requirement; quite the contrary,
- (3) applicant added *more* claims directed to pipelining to the '753 *and*
- (4) added several claims (specifically 38-43) to the present application which do not even mention pipelining at all.

Thus, both applications have been amended such that there is no longer any patentable distinction between the two sets of claims. Thus, a provisional obviousness-type double patenting rejection is deemed proper.

The following are situations where the prohibition of double patenting rejections under 35 U.S.C. 121 does not apply:

(b) The claims of the different applications or patents are not consonant with the restriction requirement made by the examiner, since the claims have been changed in material respects from the claims at the time the requirement was made. For example, the divisional application filed includes additional claims not consonant in scope to the original claims subject to restriction in the parent. *Symbol Technologies, Inc. v. Opticon, Inc.*, 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991); *Gerber Garment Technology, Inc. v. Lectra Systems Inc.*, 916 F.2d 683, 16 USPQ2d 1436 (Fed. Cir. 1990).

As of the date of this Office action, applicant has neither (1) disputed nor (2) filed a terminal disclaimer to overcome the double patenting rejection. Any response to this Office action which does not contain either of options (1) and (2) above will be held non-responsive.

Response to Amendment

9. With regard to the remarks submitted with the amendment filed July 15, 2002, these have been carefully considered but are not deemed convincing for at least the following reasons:

(A) With regard to the page 11, lines 8-12 of the remarks, applicant appears to equate "suggested" with "specifically mentioned". If this were the case, there would be no such thing as a rejection under 35 USC § 103.

(B) The examiner was not convinced by any of the arguments directed to the obviousness of data in and data out buffers associated with the DRAMs of Katayama et al. However, rather than address each of these arguments one by one, the examiner has provided as a secondary reference a compatible technology in which the use of data in and data out buffers associated with the DRAMs cannot be disputed, in order to render all of the corresponding arguments moot.

(C) As for applicant's remarks concerning the use of a plurality of memory devices (i.e., device 90), applicant's remarks hinge on the requirement that the motivation must come from the references themselves. Such motivation from has been explicitly demonstrated.

(D) Several of the examiner's comments in section 10 of the previous Office action were not addressed at all.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

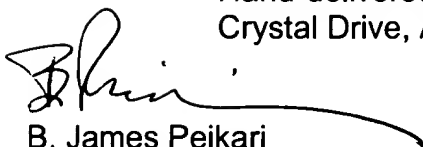
or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121
Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).



B. James Peikari
Primary Examiner
Art Unit 2186
September 7, 2002